In the Claims:

1-27. (Canceled)

28. (Currently Amended) A Fast Fourier Transform (FFT) processor for demodulating an orthogonal frequency division multiplexing (OFDM) signal including a preamble having a sequence of N samples and first data following the preamble and having a sequence of N/2 samples, the FFT processor comprising:

a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the preamble;

a controller that is configured to output a first control signal and a second control signal in response to the timing signal;

a signal converter that is configured to store the preamble in response to the first control signal, to transform the preamble by an N-point FFT into a second preamble, and to store the second preamble; ~~and~~

an FFT input buffer that is configured to store the N/2 samples of the first data while the preamble is being transformed, wherein the signal converter is further configured to perform an N-point FFT of the buffered first data and second data having a sequence of N/2 samples as the second data is sequentially received to transform the first data and the second data into third data having N samples; and

a frequency domain equalizer that is configured to synchronize the second preamble and the third data in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second preamble and the third data.

29. (Canceled)

30. (Previously Presented) The FFT processor of Claim 28, further comprising an analog to digital converter (ADC), wherein the FFT buffer is coupled to the ADC and receives the first data from the ADC and wherein the signal converter is coupled to the ADC

and receives the first data as buffered data from the FFT input buffer and receives the second data as unbuffered data from the ADC.

31. (Previously Presented) The FFT processor of Claim 30, wherein the FFT input buffer is configured to delay the first data by N/2 samples.

32. (Previously Presented) The FFT processor of Claim 30, wherein the signal converter comprises an FFT processing element including a first input line configured to receive a sample of the first data and a second input line configured to receive a sample of the second data.

33. (Previously Presented) The FFT processor of Claim 30, further comprising:

a quadrature detector that is configured to receive the OFDM signal, to convert the OFDM signal into a baseband OFDM signal, to generate a real component of the OFDM signal and an imaginary component of the OFDM signal, and to output the real component of the OFDM signal and the imaginary component of the OFDM signal to the ADC.